IN THE CLAIMS:

1. (Original) FIR filter apparatus comprising:

an input for receiving an input signal;

an FIR filter comprising a plurality of filter stages; and

a delay coupled between two of said plurality of filter stages to delay application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal.

2. (Original) Apparatus according to Claim 1, wherein the delay of said delay is adjustable.

3. (Previously Presented) FIR filter apparatus comprising:

an input for receiving an input signal;

an FIR filter comprising a plurality of filter stages,

wherein the plurality of filter stages comprises a first plurality of stages and a second plurality of stages,

the first plurality of stages receiving a predetermined first portion of the input signal; and

a delay coupled between two of said plurality of filter stages to delay application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal,

said delay providing a variable second portion of the input signal to said second plurality of stages.

4. (Original) Apparatus according to Claim 3, further comprising a memory storing a delay value for application to said delay.

5. (Original) Apparatus according to Claim 3, wherein said first plurality of filter stages comprises a plurality of filter blocks, each having a plurality of taps, and

wherein said second plurality of stages comprises at least one filter block having a plurality of taps, and

further comprising:

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks; and

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block.

6. (Original) Apparatus according to Claim 5, wherein said plurality of filter blocks comprises four filter blocks each having 32 taps, and

wherein said at least one filter block comprises one filter block having 32 taps.

7. (Original) FIR filter apparatus comprising:

a signal input receiving an input signal;

a first block of filter stages having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, for filtering a first portion of the input signal in accordance with the first plurality of weighting coefficients;

a second block of filter stages having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, for filtering a second portion of the input signal in accordance with the second plurality of weighting coefficients; and

a delay which variably delays application of the second portion of the input signal to the second block of filter stages with respect to the first portion of the input signal.

8. (Original) An FIR filter comprising:

a plurality of delay elements; and

a plurality of coefficient taps,

each associated with a portion of an input signal in corresponding stages of delay from a corresponding delay element,

wherein at least one delay element has a period of delay that is selectable.

9. (Original) An FIR filter according to Claim 8, wherein the selectable period of delay is selectable independently of a period of delay for other delay elements.

10. (Original) An FIR filter according to Claim 9, wherein each delay element has a minimum period of delay, and

wherein the selectable period of delay is adjustable to be greater than the minimum period of delay.

11. (Original) An FIR filter according to Claim 8, wherein the FIR filter further includes pin-out arrangements for setting the selectable period of delay.

12. (Original) FIR filter apparatus comprising:

input means for receiving an input signal;

filter means for filtering the input signal and having a plurality of filter stages; and

delay means coupled between two of said plurality of filter stages for delaying application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal.

13. (Original) FIR filter apparatus comprising:

signal input means for receiving an input signal;

a first block of filter means, having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, for filtering a first portion of the input signal in accordance with the first plurality of weighting coefficients;

a second block of filter means, having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, for filtering a second portion of the input signal in accordance with the second plurality of weighting coefficients; and

delay means for adjustably delaying application of the second portion of the input signal to the second block of filter means with respect to the first portion of the input signal.

14. (Original) An echo canceller comprising:

an input for receiving an input signal having an echo;

an FIR filter including:

(i) a first plurality of filter stages comprising a plurality of filter blocks, each having a plurality of taps; and

(ii) a second plurality of stages comprising at least one filter block having a plurality of taps;

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks;

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block to filter said echo; and

a delay coupled between said plurality of filter blocks and said at least on filter block to delay application of the input signal to said at least one filter block to skip filtering a portion of the input signal which contains negligible echo.

15. (Previously Presented) An Ethernet transceiver, comprising:

an input for inputting an input signal into an Ethernet cable;

an output for outputting an output signal from the Ethernet cable,

the output signal corresponding to the input signal and having an echo;

an FIR filter including:

(i) a first plurality of filter stages comprising a plurality of filter blocks, each having a plurality of taps; and

(ii) a second plurality of stages comprising at least one filter block having a plurality of taps;

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks;

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block to filter said echo; and

a delay coupled between said plurality of filter blocks and said at least one filter block to delay application of the output signal to said at least one filter block to skip filtering a

portion of the output signal which contains negligible echo.

16. (Original) A transceiver according to Claim 15, wherein said first plurality of LMS engines includes:

a first set of LMS engines applying weighting coefficients to a first filter block; and

a second set of LMS engines respectively applying weighting coefficients to a corresponding number of filter blocks.

17. (Original) A method for controlling an FIR filter comprising the steps of:

receiving an input signal;

filtering the input signal with an FIR filter having a plurality of filter stages; and

delaying application of the input signal to at least one of said filter stages with respect to the other filter stages to skip filtering a portion of the input signal.

18. (Original) A method of controlling an FIR filter comprising the steps of:

receiving an input signal;

filtering a first portion of the input signal with a first block of filter stages having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, the first portion of the input signal being filtered in accordance with the first plurality of weighting coefficients;

filtering a second portion of the input signal with a second block of filter stages having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, the second portion of the input signal being filtered in accordance with the second plurality of weighting coefficients; and

adjustably delaying application of the second portion of the input signal to the second block of filter stages with respect to the first portion of the input signal.

19. – 46. (Canceled)

IN THE DRAWINGS:

Kindly substitute Figure 2 of the above-identified application with the enclosed one (1) sheet of formal drawings of Figure 2, the sheet marked "REPLACEMENT SHEET".